Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **CLR1**
2. **D1**
3. **CLK1**
4. **PR1**
5. **Q1**
6. **N.Q1**
7. **GND**
8. **N.Q2**
9. **Q2**
10. **PR2**
11. **CLK2**
12. **D2**
13. **CLR2**
14. **VCC**

**.044”**

**.048”**

**2 1 14 13 12**

**11**

**10**

**5 6 7 8 9**

**3**

**4**

**DIE ID**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: C**

**APPROVED BY: DK DIE SIZE .044” X .048” DATE: 6/18/21**

**MFG: FAIRCHILD THICKNESS .015” P/N: 54LS74**

**DG 10.1.2**

#### Rev B, 7/19/02